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EXAMINER	
ZERVIGON, RUDY	

ART UNIT	PAPER NUMBER
1763	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,457	CONDRASHOFF ET AL.	
	Examiner	Art Unit	
	Rudy Zervigon	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *All*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5, and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Shan; Hong Ching et al. (US 5891350 A). Shan teaches an apparatus (Figure 1,3 - see common numbers) for processing a substrate ("silicon wafer"; throughout specification) with a plasma (column 2; lines 20-34), comprising: a first electrode (30; Figure 1,3; column 3; lines 34-41); a second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15) positioned with a spaced apart relationship relative to said first electrode (30; Figure 1,3; column 3; lines 34-41); a separating ring (26; Figure 3; column 9; lines 31-37) for forming a vacuum-tight seal between said first electrode (30; Figure 1,3; column 3; lines 34-41) and said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15) and defining an evacuatable processing region between said first electrode (30; Figure 1,3; column 3; lines 34-41) and said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15), said first electrode (30; Figure 1,3; column 3; lines 34-41) adapted to support the substrate ("silicon wafer"; throughout specification) in said processing region for plasma (column 2; lines 20-34) processing, and said separating ring (26; Figure 3; column 9; lines 31-37) electrically isolating said first electrode (30; Figure 1,3; column 3; lines 34-41) from said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15); a process gas port (44, Figure 1; column 3; lines 30-45) for introducing a process gas to said processing region; and a

vacuum port (50, Figure 1,3; column 3; lines 30-45) for evacuating said processing region to a pressure suitable for generating the plasma (column 2; lines 20-34) from the process gas in said processing region, as claimed by claim 1

Shan further teaches:

i. The apparatus (Figure 1,3 - see common numbers) of claim 1 further comprising: a vacuum manifold (70, Figure 4; column 15; line 62 - column 16, line25) coupled with said vacuum port (50, Figure 1,3; column 3; lines 30-45), said vacuum manifold (70, Figure 4; column 15; line 62 - column 16, line25) being electrically isolated from said first electrode (30; Figure 1,3; column 3; lines 34-41) and said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15), as claimed by claim 2

ii. The apparatus (Figure 1,3 - see common numbers) of claim 2 wherein said vacuum manifold (70, Figure 4; column 15; line 62 - column 16, line25) includes an enclosed volume proximate to said vacuum port (50, Figure 1,3; column 3; lines 30-45) and further comprising: an insert (74, 76, or 78; Figure 4; column 15; line 62 - column 16, line25) of an electrically insulating material (column 16, lines 16-25) positioned inside said enclosed volume, said insert (74, 76, or 78; Figure 4; column 15; line 62 - column 16, line25) including a first plurality of passages (72 in 74; Figure 4; column 15; line 62 - column 16, line25) coupling said vacuum manifold (70, Figure 4; column 15; line 62 - column 16, line25) with said vacuum port (50, Figure 1,3; column 3; lines 30-45), as claimed by claim 3

iii. The apparatus (Figure 1,3 - see common numbers) of claim 1 further comprising: a vacuum pump (not shown; column 13, lines 16-25) coupled with said vacuum port (50,

Figure 1,3; column 3; lines 30-45) and operative for evacuating said processing region to said pressure suitable for generating the plasma (column 2; lines 20-34) from the process gas in said processing region, as claimed by claim 5

iv. The apparatus (Figure 1,3 - see common numbers) of claim 1 further comprising a substrate holder (38; Figure 1) positioned inside said processing region and configured to support the substrate ("silicon wafer"; throughout specification) on said first electrode (30; Figure 1,3; column 3; lines 34-41), as claimed by claim 8

v. The apparatus (Figure 1,3 - see common numbers) of claim 8 wherein said substrate holder (38; Figure 1) is electrically coupled with said first electrode (30; Figure 1,3; column 3; lines 34-41), as claimed by claim 9

vi. The apparatus (Figure 1,3 - see common numbers) of claim 1 further comprising: an electrically-conductive enclosure (20; Figure 1) surrounding said separating ring (26; Figure 3; column 9; lines 31-37), said first electrode (30; Figure 1,3; column 3; lines 34-41), and said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15), said first electrode (30; Figure 1,3; column 3; lines 34-41) and said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15) each separated from said conductive enclosure (20; Figure 1) by an air gap (gas volume inside 18; Figure 1), as claimed by claim 10. Applicant's gas identity as being "air" is a claim requirement of intended use of the pending apparatus claims. Further, it has been held that claim language that simply specifies an intended use or field of use for the invention generally will not limit the scope of a claim (Walter , 618 F.2d at 769, 205 USPQ at 409; MPEP 2106). Additionally, in apparatus claims, intended use must result in a structural difference between the

claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim (In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963); MPEP2111.02).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shan; Hong Ching et al. (US 5891350 A) in view of Suntola; Tuomo et al. (US 5711811 A) and Maher, Jr.; Joseph A. et al. (US 4381965 A). Shan is disccused above. Shan does not teach:

i. An apparatus (Figure 1,3 - see common numbers) for plasma (column 2; lines 20-34) processing a plurality of substrates ("silicon wafer"; throughout specification), comprising: a first electrode (30; Figure 1,3; column 3; lines 34-41); a second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15) positioned with a spaced apart relationship relative to said first electrode (30; Figure 1,3; column 3; lines 34-41); a third electrode positioned between said first electrode (30; Figure 1,3; column 3; lines 34-41) and said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15); a first separating ring (26; Figure 3; column 9; lines 31-37) for forming a vacuum-tight seal between said first electrode (30; Figure 1,3; column 3; lines 34-41) and said third electrode and defining a first evauatable processing region between said first electrode

(30; Figure 1,3; column 3; lines 34-41) and said third electrode, said first electrode (30; Figure 1,3; column 3; lines 34-41) adapted to support one of the plurality of substrates ("silicon wafer"; throughout specification) in said first processing region for plasma (column 2; lines 20-34) processing, and said first separating ring (26; Figure 3; column 9; lines 31-37) electrically isolating said first electrode (30; Figure 1,3; column 3; lines 34-41) from said third electrode; a second separating ring (26; Figure 3; column 9; lines 31-37) for forming a vacuum-tight seal between said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15) and said third electrode to define a second evauatable processing region between said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15) and said third electrode, said third electrode adapted to support one of the plurality of substrates ("silicon wafer"; throughout specification) in said second processing region for plasma (column 2; lines 20-34) processing, and said second separating ring (26; Figure 3; column 9; lines 31-37) electrically isolating said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15) from said third electrode; at least one process gas port (44, Figure 1; column 3; lines 30-45) for introducing a process gas to said first processing region and second processing region; and a vacuum port (50, Figure 1,3; column 3; lines 30-45) for evacuating said processing region to a pressure suitable for generating the plasma (column 2; lines 20-34) from the process gas in said first processing region and said second processing space, as claimed by claim 15

ii. The apparatus (Figure 1,3 - see common numbers) of claim 15 wherein said vacuum port (50, Figure 1,3; column 3; lines 30-45) is defined in said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15), as claimed by claim 16

iii. The apparatus (Figure 1,3 - see common numbers) of claim 16 wherein said first electrode (30; Figure 1,3; column 3; lines 34-41) includes a first process gas port (44, Figure 1; column 3; lines 30-45) for introducing the process gas to said first processing region and said third electrode includes a second process gas port (44, Figure 1; column 3; lines 30-45) for introducing the process gas to said second process region, as claimed by claim 17

Suntola teaches:

iv. An apparatus (Figure 3) for plasma (column 1; lines 42-44) processing a plurality of substrates (37; Figure 3), comprising: a first separating ring (26; Figure 3; column 9; lines 31-37) for forming a vacuum-tight seal between a first chamber (38; Figure 3) and a second chamber (38; Figure 3) and defining a first evacuatable processing region (38; Figure 3) between a first chamber (38; Figure 3) and a second chamber (38; Figure 3), a first chamber (38; Figure 3) adapted to support one of the plurality of substrates (37; Figure 3) in first processing region (38; Figure 3) for plasma (column 1; lines 42-44) processing, and said first separating ring (26; Figure 3; column 9; lines 31-37) electrically isolating a first chamber (38; Figure 3) from a second chamber (38; Figure 3); a second separating ring (26; Figure 3; column 9; lines 31-37) for forming a vacuum-tight seal between a third chamber (38; Figure 3) and a second chamber (38; Figure 3) to define a second evacuatable processing region between a third chamber (38; Figure 3) and a second chamber (38; Figure 3), a second chamber (38; Figure 3) adapted to support one of the plurality of substrates (37; Figure 3) in said second processing region (38; Figure 3) for plasma (column 1; lines 42-44) processing, and said second separating ring (26;

Figure 3; column 9; lines 31-37) electrically isolating a third chamber (38; Figure 3) from a second chamber (38; Figure 3); at least one process gas port (28, 30; Figure 3) for introducing a process gas to first processing region (38; Figure 3) and second processing region (38; Figure 3); and a vacuum port (25; Figure 3) for evacuating said processing region to a pressure suitable for generating the plasma (column 1; lines 42-44) from the process gas in first processing region (38; Figure 3) and said second processing space (38; Figure 3) - claim 15

v. The apparatus (Figure 3) of claim 15 wherein said vacuum port (25; Figure 3) is defined in a third chamber (38; Figure 3), as claimed by claim 16

vi. The apparatus (Figure 3) of claim 16 wherein a first chamber (38; Figure 3) includes a first process gas port (28, 30; Figure 3) for introducing the process gas to first processing region (38; Figure 3) and a second chamber (38; Figure 3) includes a second process gas port (28, 30; Figure 3) for introducing the process gas to said second process region, as claimed by claim 17

Maher teaches a wafer plasma processing apparatus (Figure 4) including plural parallel electrodes 19a,b-25a,b each interposed between insulating dielectric layers 19c-25c.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add Suntola's apparatus (Figure 3) with Maher's plasma generating means to Shan's apparatus.

Motivation to add Suntola's apparatus (Figure 3) with Maher's plasma generating means to Shan's apparatus includes, among plural motivations, for plasma processing as taught by Suntola

(column 1; lines 42-44), and for processing plural substrates for greater through-put compared to Shan as taught by Suntola.

5. Claims 4, 6, 7, and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shan; Hong Ching et al. (US 5891350 A) in view of Hirooka; Takaaki (US 6700089 B1). Shan is discussed above. Shan does not teach:

i. The apparatus (Figure 1,3 - see common numbers) of claim 3 wherein said vacuum port (50, Figure 1,3; column 3; lines 30-45) is defined by a second plurality of passages (72 in 76; Figure 4; column 15; line 62 - column 16, line25) extending through said first electrode (30; Figure 1,3; column 3; lines 34-41) and registered with said first plurality of passages (72 in 74; Figure 4; column 15; line 62 - column 16, line25), as claimed by claim 4

ii. The apparatus (Figure 1,3 - see common numbers) of claim 1 further comprising: a process gas supply coupled with said process gas port (44, Figure 1; column 3; lines 30-45) for introducing the process gas to said processing region, as claimed by claim 6

iii. The apparatus (Figure 1,3 - see common numbers) of claim 1 wherein said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15) includes a plurality of openings arranged in a pattern effective for communicating process gas from said process gas port (44, Figure 1; column 3; lines 30-45) to said processing region, as claimed by claim 7

iv. The apparatus (Figure 1,3 - see common numbers) of claim 10 wherein said enclosure (20; Figure 1) includes a base (25; Figure 1) and a lid (24; Figure 1) movable relative to said lid (24; Figure 1) between opened and closed positions for accessing said processing

region, said lid (24; Figure 1) carrying said first electrode (30; Figure 1,3; column 3; lines 34-41) for movement relative to said base (25; Figure 1), as claimed by claim 11

v. The apparatus (Figure 1,3 - see common numbers) of claim 10 further comprising a coolant port in said lid (24; Figure 1) for supplying a flow of a coolant fluid to said air gap (gas volume inside 18; Figure 1) for cooling said first electrode (30; Figure 1,3; column 3; lines 34-41) and said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15), as claimed by claim 12

vi. The apparatus (Figure 1,3 - see common numbers) of claim 1 wherein said first electrode (30; Figure 1,3; column 3; lines 34-41) includes said vacuum port (50, Figure 1,3; column 3; lines 30-45) and said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15) includes said process gas port (44, Figure 1; column 3; lines 30-45), as claimed by claim 13

vii. The apparatus (Figure 1,3 - see common numbers) of claim 13 wherein said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15) includes a plurality of gas openings coupled with said process gas port (44, Figure 1; column 3; lines 30-45), said plurality of gas openings positioned in said second electrode (24," A_{anode}"; Figure 1,3; column 7; lines 1-15) to distribute process gas across a confronting surface of the substrate ("silicon wafer"; throughout specification), as claimed by claim 14

Hirooka teaches a plasma processing apparatus (Figure 1,2) including:

i. The apparatus (Figure 1,2) of claim 3 wherein a vacuum port (128; Figure 1,2) is defined by a second plurality of passages (126; Figure 1,2) extending through a first electrode (108+126; Figure 1) - claim 4

ii. The apparatus (Figure 1,2) of claim 1 further comprising: a process gas supply (184; Figure 2) coupled with a process gas port (194; Figure 2) for introducing the process gas to a processing region (102; Figure 2), as claimed by claim 6

iii. The apparatus (Figure 1,2) of claim 1 wherein a second electrode (124; Figure 2) includes a plurality of openings (124a; Figure 2) arranged in a pattern effective for communicating process gas from a process gas port (194; Figure 2) to a processing region (102; Figure 2), as claimed by claim 7

iv. The apparatus (Figure 1,2) of claim 10 wherein a enclosure (20; Figure 1) includes a base (104; Figure 2) and a lid (206; Figure 2,3a) movable relative to a lid (206; Figure 2,3a) between opened and closed positions for accessing a processing region (102; Figure 2), a lid (206; Figure 2,3a) carrying a first electrode (108+126; Figure 1) for movement relative to a base (104; Figure 2), as claimed by claim 11

v. The apparatus (Figure 1,2) of claim 10 further comprising a coolant port (172c; Figure 2) in a lid (206; Figure 2,3a) for supplying a flow of a coolant fluid to a air gap (172c; Figure 2) for cooling a first electrode (108+126; Figure 1) and a second electrode (124; Figure 2), as claimed by claim 12

vi. The apparatus (Figure 1,2) of claim 1 wherein a first electrode (108+126; Figure 1) includes a vacuum port (128; Figure 1,2) and a second electrode (124; Figure 2) includes a process gas port (194; Figure 2), as claimed by claim 13

vii. The apparatus (Figure 1,2) of claim 13 wherein a second electrode (124; Figure 2) includes a plurality of gas openings (124a; Figure 2) coupled with a process gas port (194; Figure 2), a plurality of gas openings (124a; Figure 2) positioned in a second

electrode (124; Figure 2) to distribute process gas across a confronting surface of the substrate ("silicon wafer"; throughout specification), as claimed by claim 14

It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace Shan's lid and lower electrode with Hirooka's lid and lower electrode.

Motivation to replace Shan's lid and lower electrode with Hirooka's lid and lower electrode is for improved hermiticity and operating speed (Hirooka:column 2; lines 10-27), and for wafer temperature control (Hirooka:column 7; lines 1-3), respectively.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Rudy Zervigon whose telephone number is (571) 272-1442. The examiner can normally be reached on a Monday through Thursday schedule from 8am through 7pm. The official fax phone number for the 1763 art unit is (571) 273-8300. Any Inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Chemical and Materials Engineering art unit receptionist at (571) 272-1700. If the examiner can not be reached please contact the examiner's supervisor, Parviz Hassanzadeh, at (571) 272-1435.

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